Public Products List

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PCN Title : STM32C031xx - product enhancement

PCN Reference : MDG/22/13524

Subject : Public Products List

Dear Customer,

There is no Standard Public Products impacted by the change

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PRODUCT/PROCESS CHANGE NOTIFICATION PCN13524 – Additional information

STM32C031xx - product enhancement

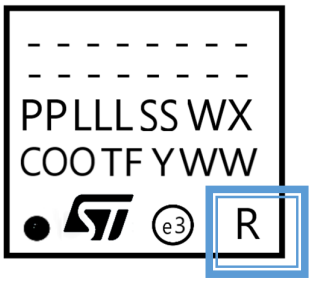
MDG – General Purpose Microcontrollers Division (GPM)

What are the changes?

Changes described in table below:

STM32C031xx	Current Cut1.0	New Cut1.1
Die revision Marking **R**	“A”	“Z”

Example: Marking on package LQFP 32L 7x7



How to order samples?

For all samples request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
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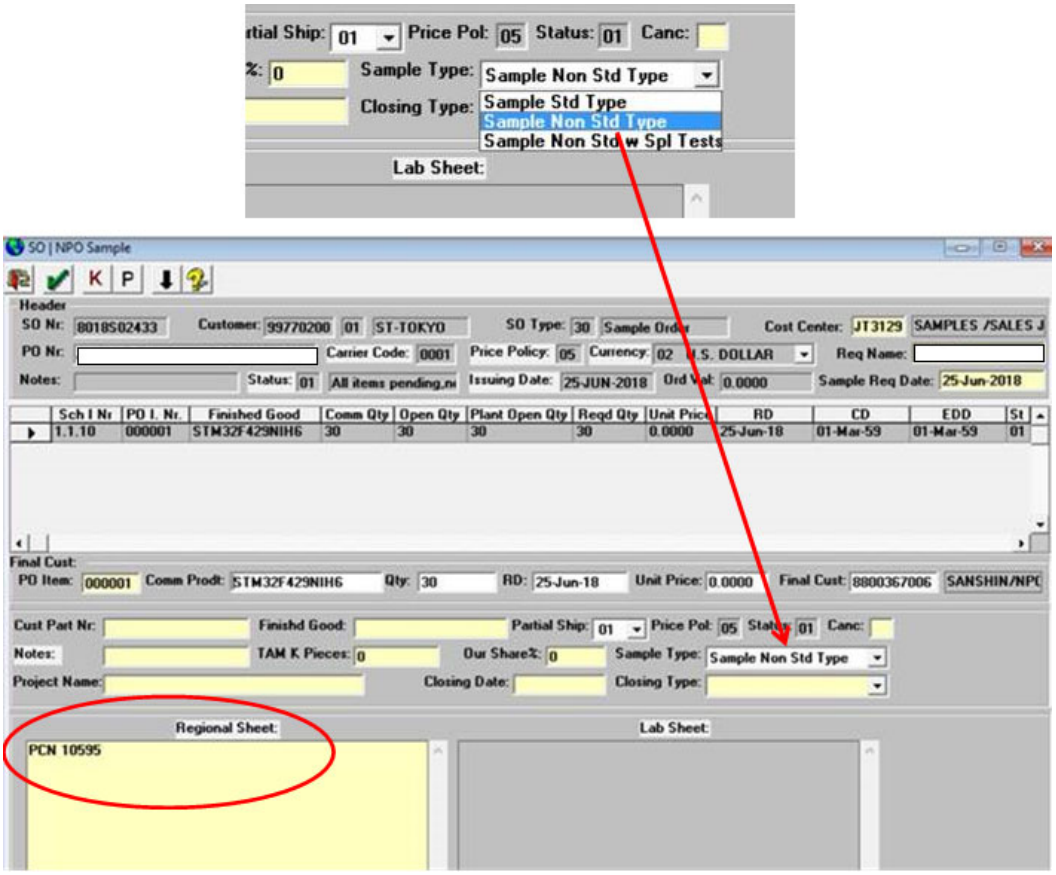
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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Reliability Evaluation Report

MDG-MCD-RER2019

STM32C031x (453x66)

Reliability Evaluation Purpose **(New Product Qualification)**

General Information	
Commercial Product	STM32C031x
Product Line	453x66
Die revision	453XXXA (Cut1.0) and 453XXXZ (Cut1.1)
Product Description	STM32C031x
Package	LQFP48 7x7, LQFP32 7x7, UFQFPN48 7x7, UFQFPN32 5x5, UFQFPN28 4x4, TSSOP20
Silicon Technology	*TSMC90 HVT FAB14*
Division	MDG-MCD
Reliability Maturity Level	*: 20->W29*

Traceability	
Diffusion Plant	TSMC Fab14, Taiwan
Assembly Plant	JSCC, China ATP1, AMKOR, Philippines ASEKH, Taiwan

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	3rd DEC 2021	Matthieu BONELLI	MDG-MCD-Q&R Engineer
1.1	18th FEB 2022	Matthieu BONELLI	MDG-MCD-Q&R Engineer
1.2	30th JUN 2022	Matthieu BONELLI	MDG-MCD-Q&R Engineer

APPROVED BY:

VERSION 1.0

Function	Location	Name	Date
BE Quality Manager	Rousset	Gisele SEUBE	8th DEC 2021
Division Q&R Responsible	Grenoble	Dominique GALIANO	9th DEC 2021
Division Quality Manager	Rousset	Pascal NARCHE	13th DEC 2021

VERSION 1.1

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	21 FEB 2022

VERSION 1.2

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	30 JUN 2022

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation performed on STM32C031x – DIE453XXXA and STM32C031x – DIE453XXXZ.

Test vehicle is described here below:

Product	Process or Package	Diffusion or Assembly plant
STM32C031C6T6	90 HVT, LQFP 7x7 48L	TSMC Fab14, JSCC
STM32C031K6T6	90 HVT, LQFP 7x7 32L	TSMC Fab14, JSCC
STM32C031C6U6	90 HVT, UFQFPN48 7x7	TSMC Fab14, JSCC
STM32C031K6U6	90 HVT, UFQFPN32 5x5	TSMC Fab14, JSCC
STM32C031G6U6	90 HVT, UFQFPN28 4x4	TSMC Fab14, JSCC
STM32C031F6P6	90 HVT, TSSOP20	TSMC Fab14, ATP1

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

The STM32C031x – Die 453XXXA and STM32C031x – Die 453XXXZ, is processed in the TSMC90 process from TSMC Fab14 Taiwan plant which is qualified through:

STM32L4x (die 415): RERMCD 1112
STM32L4x (die 435): RERMCD 1424
STM32L4x (die 462): RERMCD 1526
STM32L4x (die 461): RERMCD 1521
STM32G0 (die 460): RERMCD 1602
STM32G0 (die 466): RERMCD 1808

Based on these data, and according to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:

  Projects STM32C031x and STM32C011x are linked (Only RAM size changes. Remaining part are similar): 3 lots in total are needed for HTOL.

  Cut1.0: Full reliability exercise on 2 diffusion lots for STM32C031x and 1 diffusion lot for STM32C011x to assess the die in LQFP48 package.

  Cut1.1: Subset qualification on 1 diffusion lot for STM32C031x to assess the die in LQFP48 package.

  Note: ESD HBM & LU is done in LQFP48 (Max pin count).

- Package Qualification:

The STM32C031x (Die 453) device is assembled in the following packages already qualified for this product family:

Package	Reference	Assy Plant location
LQFP48 7x7 P0.5	RERMCD1621	JSCC
LQFP32 7x7 P0.8	RERMCD1621	JSCC
UFQFPN48 7x7 P0.5	RERMCD1622 RERMCD1808	JSCC
UFQFPN32 5x5 P0.5	RERMCD1622 RERMCD1808	JSCC
UFQFPN28 4x4 P0.5	RERMCD1623	JSCC
TSSOP20 P0.65	RERMCD1712	ATP1

The reliability test plan and result summary are presented in the following table:

Package	Body	Pitch	Package Code	Wire	Assy	Bounding Option	Trial
LQFP48	7x7	0.5	5B	Gold	JSCC	NA	1 reliability lot + CA focusses on FE/BE interface
LQFP32	7x7	0.8	5V	Gold	JSCC	NA	CDM only
UFQFPN48	7x7	0.5	A0B9	Gold	JSCC	NA	1 reliability lot + CA focusses on FE/BE interface
UFQFPN32	5x5	0.5	A0B8	Gold	JSCC	NA	CDM only
UFQFPN28	4x4	0.5	A0B0	Gold	JSCC	NA	1 reliability lot + CA focusses on FE/BE interface
TSSOP20		0.65	YA	Gold	ATP1	NA	1 reliability lot + CA focusses on FE/BE interface

For LQFP32 we can apply similarity rules with LQFP48 so only CDM needed.
For UFQFN32, only CDM needed thanks to available reliability on same packages with similar die sizes.

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the waiver 29 is granted for the STM32C031x- Die 453XXXA and STM32C031x- Die 453XXXZ for LQFP48, LQFP32, UFQFPN48, UFQFPN32, UFQFPN28, TSSOP20 packages.

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

STM32C0 family (DIE 443 & 453) is a derivated from STM32L4 family.

For additional information concerning the product behavior, refer to STM32C031x datasheet.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1	
Wafer fab name / location	TSMC Fab14 / Taiwan
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	TN090CE
Number of masks	39
Die finishing front side (passivation) materials/thicknesses	USG + NITRIDE/1.9µm
Die finishing back side Materials/thicknesses	RAW SILICON
Die area (Stepping die size) (µm)	X:1419.8µm Y:2074.2µm 2.9449 mm²
Die pad size (µm)	123, 59
Sawing street width (X,Y) (µm)	80, 80
Metal levels/Materials/Thicknesses	Rank - Metal composition - Thickness (µm) 1 - TaN/Ta/CuSeed/Cu - 0.240 / 2 - TaN/Ta/CuSeed/Cu - 0.310 3 - TaN/Ta/CuSeed/Cu - 0.310 / 4 - TaN/Ta/CuSeed/Cu - 0.310 5 - TaN/Ta/CuSeed/Cu - 0.310 / 6 - TaN/Ta/CuSeed/Cu - 0.850 7 - AlCu - 1.450
Die over coating (material/thickness)	
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	2 FITs
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	Alpha SER: 491 FIT/Mb Neutron SER: 445 FIT/Mb Neutron SER is an estimation at sea level of NYC (14n/h/cm²). Alpha result is estimated using a nominal flux of 0.001α/h/cm²
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI) - Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	Yes
Other Device(s) using same process	STM32G0x, STM32L4x, STM32G4x product family, 415, 435, 461, 462, 464, 470, 468, 469, 466, 479

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 – LQFP 7x7x1.4 48L 5B	
Assembly plant name / location	STATSChipPAC SCCJ / SC-StatsChippac-China (SCCJ)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375±25
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/reference	LQFP48L 184sq Eff slots pur tin STMP LF JSCC
Lead frame finishing (material/thickness)	Pure Tin (e3): tolerance 7 to 20 µm
Die attach material/type glue	D/A Ablestik 3230
Wire bonding material/diameter	Gold Wire/0.8mil
Molding compound material/supplier/reference	Mold Sumitomo low alpha G631SHQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3
Package 2 – LQFP 7x7x1.4 32L 5V	
Assembly plant name / location	STATSChipPAC SCCJ / SC-StatsChippac-China (SCCJ)
Pitch (mm)	0.8
Die thickness after back-grinding (µm)	375±25
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/reference	LQ7 32L 184sq Eff slots STMP LF JSCC
Lead frame finishing (material/thickness)	Pure Tin (e3): tolerance 7 to 20 µm
Die attach material/type glue	D/A Ablestik 3230
Wire bonding material/diameter	Gold Wire/0.8mil
Molding compound material/supplier/reference	Mold Sumitomo low alpha G631SHQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3
Package 3 – UFQFPN 7x7x0.55 48L A0B9	
Assembly plant name / location	STATS ChipPAC/ China (SCCJ)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150±25
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/reference	Rough Cu LF UQFN48L 5.2sq Groove JSCC
Lead frame finishing (material/thickness)	Pure Tin (e3): tolerance 7 to 20 µm
Die attach material/type glue	Glue Hitachi EN4900GC
Wire bonding material/diameter	Gold Wire/0.8mil
Molding compound material/supplier/reference	RESIN SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3

Package 4 – UFQFPN 5X5X0.55 32L A0B8	
Assembly plant name / location	STATS ChipPAC/ China (SCCJ)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150±25
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/reference	HD LF FOR UQFN 5x5 32L Sn PAD 3.1 MM SQ Groove
Lead frame finishing (material/thickness)	Pure Tin (e3): tolerance 7 to 20 µm
Die attach material/type glue	Glue Hitachi EN4900GC
Wire bonding material/diameter	Gold Wire/0.8mil
Molding compound material/supplier/reference	RESIN SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3
Package 5 – UFQFPN 4X4X0.55 28L A0B0	
Assembly plant name / location	STATS ChipPAC/ China (SCCJ)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150±25
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/reference	LF UQFN4x4 COL 020614H uPPF3L 4UP JSCC
Lead frame finishing (material/thickness)	Pure Tin (e3): tolerance 7 to 20 µm
Die attach material/type film	DAF HITACHI HR-5104T-25
Wire bonding material/diameter	Gold Wire/0.8mil
Molding compound material/supplier/reference	MOLD COMPOUND SUMITOMO EME G770HCD
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3
Package 6 – TSSOP 20 BODY 4.4 YA	
Assembly plant name / location	ATP1 AMKOR/Philippines
Pitch (mm)	0.65
Die thickness after back-grinding (µm)	275±25
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/reference	TSSOP20 2.4x3.6 2sRough CuLF SID101403921
Lead frame finishing (material/thickness)	Pure Tin (e3): tolerance 7 to 20 µm
Die attach material/type glue	GLUE D/A ABLESTIK 8290
Wire bonding material/diameter	Gold Wire/0.8mil
Molding compound material/supplier/reference	Resin Sumitomo EME-G700LS
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	RCCAL / ROUSSET GRAL / GRENOBLE

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	9R115536/ WAFER#11	1.0	GQ1242BF	705B*453ESXA	LQFP 7x7 48L	Die and Package Reliability assessment
2	9R111492/ WAFER#24	1.0	GQ1242BE	705B*453ESXA	LQFP 7x7 48L	Die Reliability assessment
3	9R117550/ WAFER#24	1.0	GQ1282A8	705B*443ESXA	LQFP 7x7 48L	Die Reliability assessment
4	9R115536/ WAFER#11	1.0	GQ128200	705V*453ESXA	LQFP 7x7 32L	Package Reliability assessment
5	9R115536/ WAFER#9	1.0	GQ128201	70MB*453ESXA	UFQFPN 7x7 48L	Package Reliability assessment
6	9R115536/ WAFER#12	1.0	GQ128203	70MG*453ESXA	UFQFPN 5x5 32L	Package Reliability assessment
7	9R115536/ WAFER#9	1.0	GQ127202	70MB*453ESXA	UFQFPN 4x4 28L	Package Reliability assessment
8	9R115536/ WAFER#10	1.0	7B126464	P0YA*453ESXA	TSSOP20	Package Reliability assessment
9	9R116515/ WAFER#13	1.1	GQ21524C	705B*453ESXZ	LQFP 7x7 48L	DIE Reliability assessment

3.2 Test plan and results summary

Table 5 – ACCELERATED LIFETIME SIMULATION TESTS

For LQFP 7x7 48L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 1200H 3V6	2	77	144	Lot1: 0/77 Lot2: 0/77	
		Ta=125°C Duration= 600H 3V6	2	77	144	Lot3 : 0/77 Lot9 : 0/77	*Lot 3 using die443, STM32C011x product*
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class2	2	3	6	Lot1: 0/3 Lot9: 0/3	
LatchUp	JESD78	130°C	2	3	6	Lot1:0/3 Lot9:0/3	
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C – Duration 1500H	1	77	77	Lot1: 0/77	
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C – Duration 168H	1	77	77	Lot9: 0/77	
EDR	JESD22-A117	10kcy EW @ 25°C then Storage HTB 150°C – Duration 168h	1	77	77	Lot1: 0/77	
EDR	JESD22-A117	10kcy EW @ -40°C then Storage HTB 150°C – Duration 168H	1	77	77	Lot1: 0/77	
ELFR	JESD22-A108 JESD74	Ta=125°C Duration= 48hrs 3V6	3	500	1500	Lot1: 0/500 Lot2: 0/500 Lot9: 0/500	

Table 6 – ACCELERATED ENVIRONMENT STRESS TESTS

Note: Test method revision reference is the one active at the date of reliability trial execution

LQFP7x7 48L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	2	3	6	Lot1: 0/3 Lot9: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot1: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot1: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot1: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot1: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot1: 0/77	
CA	Construction Analysis including -Wire bond shear -Wire bond pull	internal ST Specs	1	50	50	Lot1 : 0/50	

LQFP7x7 32L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot4: 0/3	

UFQFPN7x7 48L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot5: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot5: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot5: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot5: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot5: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot5: 0/77	
CA	Construction Analysis including -Wire bond shear -Wire bond pull	internal ST Specs	1	50	50	Lot5: 0/50	

UFQFPN5x5 32L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot6: 0/3	

UFQFPN4x4 28L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot7: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot7: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot7: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot7: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot7: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot7: 0/77	
CA	Construction Analysis including -Wire bond shear -Wire bond pull	internal ST Specs	1	50	50	Lot7: 0/50	

TSSOP20, ATP1

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot8: 0/3	
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot8: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot8: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot8: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot8: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot8: 0/77	
CA	Construction Analysis including -Wire bond shear -Wire bond pull	internal ST Specs	1	50	50	Lot8: 0/50	

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Temperature Humidity Bake
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Matthieu BONELLI	Initial Release	Div. Quality Manager	Rousset	Pascal NARCHE	13th DECEMBER 2021
			Q&R Quality Manager	Grenoble	Dominique GALIANO	9th DECEMBER 2021
			BE Quality Manager	Rousset	Gisele SEUBE	8th DECEMBER 2021
1.1	Matthieu BONELLI	Add results of UFQFPN48, UFQFPN32, UFQFPN28 and TSSOP20	Q&R Quality Manager	Grenoble	Dominique GALIANO	21rst FEBRUARY 2022
1.2	Matthieu BONELLI	Add results of cut1.1	Q&R Quality Manager	Grenoble	Dominique GALIANO	30th June 2022

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